

**Electronic Assembly With Sandwiched Capacitors  
And Methods of Manufacture**

5

**Abstract of the Disclosure**

To provide high-speed, low inductance capacitive decoupling, an integrated circuit (IC) package includes capacitors positioned within the mounting region between a die and an IC package substrate. A variety of types and sizes of capacitors and substrates can be employed in a variety of geometrical arrangements. In some embodiments, capacitors are sandwiched between die terminals or bumps and the substrate conductors or pads, while in other embodiments, capacitors are positioned between bar-type conductors on the surface of the IC package substrate. Methods of fabrication, as well as application of the package to an electronic assembly and to an electronic system, are also described.

RECEIVED  
U.S. POSTAL SERVICE  
MAY 15 2001

"Express Mail" mailing label number: EV041119662US

Date of Deposit: December 3, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to U.S. Patent and Trademark Office, Box Patent Application, P.O. Box 2327, Arlington, VA 22202.